DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Steven Capella on 07/17/2008.

3. The application has been amended as follows:

1. (currently amended) A circuit, comprising: a control circuit [[adapted]] configured to generate at least a first and second signal in response to a test enable signal; a differential driver circuit coupled to said control circuit, having a differential input node and a differential output node and [[adapted]] configured to receive a differential input signal at said differential input node, amplify said differential input signal and transmit a differential output signal onto said differential output node in response said first signal, said differential driver circuit further comprising: a plurality of [[FIR]] finite-impulse-response (FIR) latches coupled to said differential input node and [[adapted]] configured to store said differential input signal; a plurality of preamplifier circuits coupled to said FIR latches and [[adapted]] configured to amplify said differential input signal, wherein said preamplifier circuits are enabled in response to said first signal; a driver output stage coupled to said preamplifier circuits and [[adapted]]

configured to transmit said differential output signal; and a current [[DAC]] digital-to-analog (DAC) circuit coupled to said driver output stage and [[adapted]] configured to set drive strength of said driver output stage in response to a plurality of [[IDAC]] current digital-to-analog converter (IDAC) control signals; a programmable termination impedance circuit coupled to said control circuit and said differential output node, [[adapted]] configured to generate a differential termination impedance at said differential output node in response to said second signal; and a differential receiver circuit coupled to said control circuit and said differential output node, [[adapted]] configured to receive said differential output signal, convert said differential output signal to a single ended signal and transmit said single ended signal in response to said test enable signal.

2. (original) The circuit of claim 1 further comprising: a first shift-register-latch circuit coupled to said differential input node and [[adapted]] configured to store said differential input signal; and a second shift-register-latch circuit coupled to said differential receiver circuit and [[adapted]] configured to store said transmitted single ended signal.

5. (currently amended) The circuit of claim 3 claim 1, further comprising a third shift-register-latch circuit coupled to said current DAC circuit and [[adapted]] configured to store said IDAC control signals.

12. (currently amended) The circuit of claim 1 1claim 22, wherein said differential receiver further comprises a second built-in offset voltage comparator circuit electrically coupled in parallel with said first built-in offset voltage comparator

circuit and [[adapted]] configured to output a signal in response to said differential output signal and a second offset voltage, wherein said first built-in offset voltage comparator circuit and said second built-in offset voltage comparator circuit form a hysteresis comparator.

21. (new) A circuit, comprising: a control circuit [[adapted]] configured to generate at least a first and second signal in response to a test enable signal; a differential driver circuit coupled to said control circuit, having a differential input node and a differential output node and [[adapted]] configured to receive a differential input signal at said differential input node, amplify said differential input signal and transmit a differential output signal onto said differential output node in response said first signal; a programmable termination impedance circuit coupled to said control circuit and said differential output node, [[adapted]] configured to generate a differential termination impedance at said differential output node in response to said second signal, said programmable termination impedance circuit comprises a plurality of resistor components, each resistor component having an associated switch for selectively connecting that resistor component from a voltage source to said differential output node, wherein at least one, but less than all of said resistor components are coupled to a first node of said differential output node and a remainder of said resistor components are coupled to a second node of said differential output node; and a differential receiver circuit coupled to said control circuit and said differential output node, [[adapted]] configured to receive said differential output signal, convert said differential

output signal to a single ended signal and transmit said single ended signal in response to said test enable signal.

22. (new) A circuit, comprising: a control circuit [[adapted]] configured to generate at least a first and second signal in response to a test enable signal; a differential driver circuit coupled to said control circuit, having a differential input node and a differential output node and [[adapted]] configured to receive a differential input signal at said differential input node, amplify said differential input signal and transmit a differential output signal onto said differential output node in response said first signal; a programmable termination impedance circuit coupled to said control circuit and said differential output node, [[adapted]] configured to generate a differential termination impedance at said differential output node in response to said second signal; and a differential receiver circuit coupled to said control circuit and said differential output node, [[adapted]] configured to receive said differential output signal, convert said differential output signal to a single ended signal and transmit said single ended signal in response to said test enable signal, said differential receiver circuit comprising: a differential amplifier circuit coupled to said differential output node and [[adapted]] configured to receive said differential output signal; a built-in offset voltage comparator circuit coupled to said differential amplifier circuit and [[adapted]] configured to output a signal in response to said differential output signal and an offset voltage; an output stage coupled to said differential amplifier circuit and said built-in offset voltage comparator circuit and [[adapted]] configured to transmit said single ended signal

in response to said output signal of said built-in offset voltage comparator circuit; and a level shifter circuit coupled to said output stage and [[adapted]] configured to transition power supply domains from an analog power supply domain to a digital power supply domain.

Allowable Subject Matter

4. Claims 1-2, 4-5, 8-10, 12-15 and 21-22 are allowed.

5. The following is an examiner's statement of reasons for allowance: the prior art of record, taken alone or in combination, fails to disclose or render obvious, a circuit, comprising: a control circuit, a differential driver circuit comprising: a plurality of finite-impulse-response (FIR) latches coupled to said differential input node and configured to store said differential input signal; a plurality of preamplifier circuits coupled to said FIR latches and configured to amplify said differential input signal, wherein said preamplifier circuits are enabled in response to said first signal; a driver output stage coupled to said preamplifier circuits and configured to transmit said differential output signal; and a current digital-to-analog (DAC) circuit coupled to said driver output stage and configured to set drive strength of said driver output stage in response to a plurality of current digital-to-analog converter (IDAC) control signals; a programmable termination impedance circuit coupled to said control circuit and said differential output node; and a differential receiver circuit coupled to said control circuit and said differential output node, in combination with all the limitations of recited in claim 1;

a circuit comprising: a control circuit, a differential driver circuit coupled to said control circuit, a programmable termination impedance circuit coupled to said control

circuit and said differential output node, configured to generate a differential termination impedance at said differential output node in response to said second signal, said programmable termination impedance circuit comprises a plurality of resistor components, each resistor component having an associated switch for selectively connecting that resistor component from a voltage source to said differential output node, wherein at least one, but less than all of said resistor components are coupled to a first node of said differential output node and a remainder of said resistor components are coupled to a second node of said differential output node; and a differential receiver circuit coupled to said control circuit and said differential output node, in combination with all the limitations of recited in claim 21;

a circuit comprising: a control circuit, a differential driver circuit coupled to said control circuit, a programmable termination impedance circuit coupled to said control circuit and said differential output node, a differential receiver circuit coupled to said control circuit and said differential output node, said differential receiver circuit comprising: a differential amplifier circuit coupled to said differential output node and configured to receive said differential output signal; a built-in offset voltage comparator circuit coupled to said differential amplifier circuit and configured to output a signal in response to said differential output signal and an offset voltage; an output stage coupled to said differential amplifier circuit and said built-in offset voltage comparator circuit and configured to transmit said single ended signal in response to said output signal of said built-in offset voltage comparator circuit; and a level shifter circuit coupled to said output stage and configured to transition power supply domains from an analog power supply

domain to a digital power supply domain, in combination with all the limitations of recited in claim 22.

Claims 2, 4-5, 8-10 and 12-15 depending from claims 1, 21 or 22 are allowed for the same reason.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am- 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Examiner, Art Unit 2829
07/17/2008

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